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## **InPA Systems and S2C Partner to Enhance Rapid Prototype Debug Flow**

*Technology to be demonstrated at SoCIP 2011  
Shanghai 5/24 Beijing 5/26*

San Jose, California – May 16, 2011 - [InPA Systems, Inc.](#), an innovator in FPGA-based rapid prototyping bring up and debug and [S2C Inc.](#), a leading rapid SoC/ASIC prototyping solutions provider, announced today that they have partnered for the development and testing of an integrated solution for high-speed, multi-FPGA debug. This technology is still in beta, but it is expected to be released in Q3 2011. InPA will demonstrate the integrated technology with the S2C hardware at the InPA Systems booth at [SoCIP 2011](#) and at the Design Automation Conference (DAC) 2011 in June (Booth #3216).

How do the two technologies integrate? InPA utilizes the S2C I/O connector to access user FPGA signals and the S2C LM controller FPGA that is on the [V6 TAI Logic Module](#). The unique benefit of this partnership is that, because the InPA technology shares the same LM controller FPGA on the S2C TAI Logic Module, the user does not need a separate board to control the high-speed multi-FPGA trigger and capture debug activity.

“We are pleased to offer our SoC/ASIC prototyping customers a new advanced Multi-FPGA debug capability by supporting the InPA technology,” said Mon-Ren Chene, Chairman and CTO of S2C Inc. “Combining the InPA debug tools with our V6 TAI Logic Module, our customers can enjoy high speed powerful multi-FPGA debug with our proven 4<sup>th</sup> generation prototyping hardware to reduce design implementation iterations in FPGAs.”

“S2C has been instrumental in testing and helping integrate our technologies,” said Michael Chang, CEO at InPA Systems, “The debug of today’s SoCs on multi-FPGA prototype systems is daunting to say the least. Our aim is to make this process much more efficient with a combination of methodology and advanced technology.”

InPA Systems came on the scene last August when it announced the formation of its company. InPA’s *Active Debug*<sup>™</sup> technology allows users unprecedented visibility and control of the verification and validation process when integrating SoC software and hardware onto multi-FPGA prototype systems. What is the primary benefit to users? A drastic reduction in FPGA implementation iterations when trying to detect a HW/SW integration issue when using multi-FPGA prototype systems.

For more information on this integrated technology see [www.inpasystems.com/partners/hardware](http://www.inpasystems.com/partners/hardware) or drop by the InPA Systems booth at the SoCIP 2011 show in Shanghai and Beijing or at booth#3216 at DAC for a demonstration.

#### ***About InPA Systems***

InPA is an innovator in FPGA-based rapid prototyping bring up and debug. The company integrates RTL simulation with FPGA prototype hardware, provides at-speed *Active Debug*<sup>™</sup> technology and a zoom in/out methodology into the multi-FPGA prototype to compress the time it takes to debug the hardware/software integration of SoC designs. Privately held and funded, InPA was founded in 2007 in San Jose.

Its corporate headquarters is at 22 Great Oaks Blvd. Suite 280, San Jose, CA 95119-1457, phone: (408) 362-1541, fax: (408) 362-9087. On the Web at: [www.inpasystems.com](http://www.inpasystems.com)

#### ***About S2C Inc.***

Founded and headquartered in San Jose, California, S2C has been successfully delivering rapid SoC prototyping solutions since 2003. S2C provides:

- Rapid SoC FPGA-based prototyping hardware and automation software
- Prototype Ready<sup>™</sup> IP, Platforms, and Accessories
- System-level design verification and acceleration

S2C's value is our singular focus on SoC/ASIC development. Our highly qualified engineering team and customer-focused sales force understands our customers’ SoC development needs. S2C’s unique FPGA-based solution, using our patented TAI IP technology, enables designers to quickly assemble FPGA-based SoC prototypes on S2C FPGA boards. This gives customers an early start on software development, typically the long pole item in development schedules. Combining rapid prototyping methodologies with a comprehensive portfolio of Prototype Ready IP and advanced verification and acceleration solutions, S2C solutions greatly reduces the SoC design cycle.

In addition to the headquarters in San Jose, CA, S2C currently has 4 direct offices located in Shanghai, Beijing, Shenzhen China and HsinChu, Taiwan. S2C is also the organizer of the annual [SoCIP](#) seminar and exhibition in China, which brings SoC designers from the Asia-Pacific region together with international silicon IP and SoC solution vendors. For more information, visit [www.s2cinc.com](http://www.s2cinc.com) .

***About V6 TAI Logic Module***

The V6 TAI Logic Modules are S2C's fourth generation SoC/ASIC prototyping hardware and can be configured with one or two Xilinx Virtex-6 760 or 550 FPGA devices on one board to fit for ASIC/SoC designs ranging from 5.5M to 15.2 million ASIC gates. The V6 TAI Logic Module has enhanced power management, noise shielding, and cooling mechanism that enables system prototypes to attain higher performance and reliability. The V6 TAI Logic Modules can run both DDR2 memory at up to 600MHz and DDR3 memory at up to 800Mbps using on-board SO-DIMM sockets. Users can easily download FPGAs, generate programmable clocks, and self-test hardware from S2C's TAI Player Software via a USB2.0 port.

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*Note: Active Debug™ is a trademark of InPA Systems, Inc. S2C, Prototype Ready, and TAI, are trademarks of S2C, Inc. All other trademarks and registered trademarks are the property of their respective owners.*