



For more information, contact:

Joe Gianelli (joe@inpasystems.com)
InPA Systems
831-252-6418

Liz Massingill (liz@leepr.com)
Lee PR
650-363-0142

InPA Systems Inc. Targets *Active Debug*[™] for Rapid Prototyping

San Jose, California – August 16, 2010 - [InPA Systems, Inc.](#) has been formed to develop and market [FPGA-based rapid prototyping](#) technology that allows users to employ the company's patent pending [Active Debug](#) including full visibility technology to better detect hardware faults and reduce the FPGA P&R iterations associated with the debug cycle for next-generation complex SoCs.

InPA's *Active Debug* technology allows users unprecedented visibility and control of the verification and validation process when integrating software and hardware onto SoC designs, a major technological leap in reducing today's highly iterative process of "blind" or passive probing required when using current prototyping debug methods.

"We use FPGA prototypes extensively for our SoC design projects as it has become an essential hardware verification and software application validation tool," said Dr. Gene Chuang, SoC Technical Director, Wireless Broadband Technology Division of ITRI in Taiwan.

Chuang continued, "While FPGA prototypes are popular, they are also difficult to use. We are excited to see that the InPA Systems *Active Debug* including full visibility technology will make our FPGA prototype verification environment even more powerful and easy to use and look forward to using their product when it's released."

InPA Systems was founded in October 2007 by two longtime EDA entrepreneurs: noted logic emulation authority [Thomas Huang](#), who is chairman and CTO; and verification expert [Michael Chang](#), who is president and CEO. Both Huang and Chang have founded a number of startups and bring a wealth of expertise in logic emulation, rapid prototyping and verification to InPA. They hold ten patents in the areas of logic emulation and equivalence checking.

InPA Systems is privately funded and has recruited a board of key advisors with vast and noteworthy academic, EDA and IC design industry credentials and expertise. Along with Huang and Chang, outside advisors are: [Bernie Aronson](#), former CEO or president of companies such as Kilopass, Synplicity and Epic; and [Michel Courtoy](#), former CEO at Certess, [Sean Torsney](#), former VP of marketing and sales at Verplex and currently VP marketing and sales at VisualOn, and

[Kazuyuki Kawauchi](#), held senior management positions at Fujitsu Semiconductor Limited in Japan and at Fujitsu Microelectronics America and is currently president of D₂S KK.

InPA Systems is entering into one of the fastest growing EDA segments--rapid prototyping. According to InPA estimates, the rapid prototype sub-segment of the EDA market has had a CAGR of better than 20% over the last 5 years and is poised to grow even faster over the next couple of years. InPA believes that more new technology and attention will be focused on this sub-segment in the near future, making FPGA prototypes even more popular.

Technology differentiation

The key to InPA Systems' next generation rapid prototyping debug product is its *Active Debug* including full visibility technology. For the first time, users gain control when running the design, at speed, in the validation process, allowing them to capture complex scenarios in the FPGAs and analyze system faults with full signal visibility. Current passive debug technology requires a highly iterative and mostly, blind process that requires the user to continually guess where system faults might be located on the SoC. The primary benefit of *Active Debug* including full visibility technology is that it compresses the time it takes to integrate hardware and software and to debug SoC designs.

"It's become obvious to most all SoC design teams that FPGA-based prototype boards are invaluable when verifying the hardware and validating software applications in system," said Mike Dini, CEO of The Dini Group. "What's been missing is the ability to efficiently debug a multi-FPGA system. We champion InPA Systems' efforts to bring their *Active Debug* including full visibility technology to market to vastly improve the way our multi-FPGA systems are debugged."

Executive team

Huang is probably best known as a co-founder and the CTO of PiE Design Systems, a pioneering logic emulation company. He joined Quickturn when that company acquired PiE. Huang was also EVP and CTO of Aptix, a rapid prototyping company and founded several other companies in the emulation and ATE areas. He holds nine patents covering various aspects of logic emulation.

Chang is the highly-regarded co-founder, CEO and president of Verplex, a formal verification company that was acquired by Cadence. He spent a number of years at Cadence as VP and GM of the formal verification group there. Chang also founded DFT vendor Checklogic that was acquired by Mentor Graphics and holds a patent in equivalence checking.

[Joe Gianelli](#) is vice president of marketing and business development. Gianelli joined InPA after a successful launch and acquisition of Taray Inc. Before that he spent a decade-long stint at Synplicity, Inc., where he joined its executive staff as VP business development. Gianelli is a veteran of the EDA industry, having held technical and business positions at Synopsys, Epic Design Technology, Meta Software, and Cadence Design Systems.

Ecosystem and product

InPA is in the process of building its partnership ecosystem with EDA and FPGA prototype providers and key distribution companies who are focused on the rapid prototype market segment, so that the company can offer customers a completely integrated product. These partnerships will be announced over the next few months. The company expects its first product to be available in 4Q 2010.

About InPA Systems

InPA is an innovator in the debug of FPGA-based rapid prototyping. The company integrates RTL simulation, hardware and software debug environments, provides an *Active Debug* methodology and enables full visibility into the multi-FPGA prototype to compress the time it takes to debug SoC designs. Privately held and funded, InPA was founded in 2007 in San Jose. Its corporate headquarters is at 22 Great Oaks Blvd. Suite 280, San Jose, CA 95119-1457, phone: (408) 362-1541, fax: (408) 362-9087. On the Web at: <http://inpasystems.com/>

– end –

Note: Active Debug is a trademark of InPA Systems, Inc. All other trademarks and registered trademarks are the property of their respective owners